Amendments to the Specification:

Please amend paragraph number **[0002]** as follows:

[0002] State of the Art: The manufacture of semiconductor devices, commonly termed "dice" or "chips," encompasses a plurality of major manufacturing stages, each of which typically comprises a number of elements. In general, chip manufacture may be generalized as comprising the stages of crystal growth, wafer preparation, wafer fabrication, wafer sort, and packaging. Wafer sort and packaging may be performed in a different order, or combined into a single manufacturing stage. Typically, a wafer of a semiconductor material such as silicon is cut from a large crystal and may have a nominal diameter of up to about 300 mm (12 inches). Although larger bulk semiconductor substrates may have been fabricated, the 300 mm wafer is the largest-size wafer currently being phased into commercial production runs by various semiconductor device manufacturers. As cut from a cylinder of semiconductor material transverse to the longitudinal axis thereof, a wafer typically has a thickness considerably greater than the usual end product of the semiconductor fabrication, i.e., singulated semiconductor dice. While a designated active surface of a wafer is repeatedly planarized following applications of various material layers during the fabrication of integrated circuitry thereon, the ~~back~~back side surface is generally left relatively rough, requiring a bulk material removal operation to remove extraneous material to thin the wafer and, optionally, a planarization step to reduce the roughness of the ~~back~~back side surface. For example, a wafer having an initial thickness prior to fabrication of integrated circuitry thereon of about 28 mils may be thinned to a final thickness of about 4 mils.

Please amend paragraph number **[0003]** as follows:

[0003] The fabrication stage of IC production is concentrated on the "active" surface of the wafer, which is relatively planar. Electrical components such as transistors, resistors, capacitors and the ~~like,~~ like; as well as interconnecting conductors, i.e., ~~metallization,~~ metallization; are formed on the active surface during the wafer fabrication stage. On the other hand, the role of the ~~back~~ back side surface of the wafer, if any, is typically that of a mounting surface used to attach an individual semiconductor die to a carrier substrate of some sort. For

example, the ~~back~~back side of a semiconductor die may be attached to a lead frame paddle, to an interposer, to a circuit board, to another die, or to some other substrate. In other instances, such as in the case of leads-over-chip packaging or in certain chip-scale packaging configurations, the ~~back~~back side of a semiconductor die may be encapsulated or merely coated. However, as package sizes have decreased, reduction in die (and thus wafer) thickness has been emphasized to reduce the thickness of the resulting packaged electronic device. Wafer thinning and planarization of the ~~back~~back side are required to reduce the wafer thickness to a desired dimension and provide a desired surface smoothness. The continual goal of producing integrated circuits of greater density (memory or logic components per unit volume) necessitates that semiconductor dice be of minimal thickness while retaining sufficient resistance to breakage, warping, electrical degradation and dislocation formation. It is anticipated that reducing wafer thickness to the range of 2 mils or less will become commercially feasible in the near future.

Please amend paragraph number **[0006]** as follows:

[0006] When conventional material removal ~~techniques~~ techniques, such as those referenced ~~above~~ above, are applied to the thinning and planarization of a wafer ~~back~~back side, deficiencies are exhibited due to the initial roughness and nonplanarity of the ~~back~~back side surface produced when the wafer is severed from the cylinder of semiconductor material. Chemical thinning processes, e.g., wet etches and dry etches, remove substrate material at substantially the same rate in a direction normal to the surface, whether the surface portion in question is on a "peak" or in a "valley." Thus, the finally thinned surface will have a generally similar topography but with reduced amplitude. In this application, "amplitude" is defined as the vertical distance between the point of greatest penetration from a mean surface level and the point of greatest elevation above the mean surface level.

Please amend paragraph number **[0007]** as follows:

[0007] In the case of a physical thinning process, e.g., abrasive grinding, it has been found that the lateral abrasive forces impinging upon the sides of "peaks" and "valleys" cause fracture and breakage below the valley levels. High-asperity-induced particles are produced,

leading to further nonuniformities in removal rate. In addition, backgrinding wafers using conventional diamond grinding wheels may exacerbate the occurrence of flaws in the ~~back~~back side of a wafer.

Please amend paragraph number **[0008]** as follows:

[0008] It is desirable that the ~~back~~back side surface of the substrate be carefully thinned in a planar manner thereacross, particularly when nearing the end point of the thinning operation wherein a final substrate thickness is reached. However, localized stresses may cause wafer cracking, breakage, warpage and the like, particularly in the case of a very thin substrate. The thinning process is complicated by any warpage of the wafer occurring responsive to internal substrate stresses as the wafer is thinned. Such warpage may cause nonplanarity of the ~~back~~back side surface as thinning continues and is difficult to compensate for. As wafers are thinned to an ever-greater extent, the tendency to warp is exacerbated as stresses induced by fabrication of the integrated circuitry on the active surface of the wafer become more significant.

Please amend paragraph number **[0010]** as follows:

[0010] The thinning and planarizing of the ~~back~~back side of a semiconductor wafer and the like by conventional techniques leaves much to be desired, inasmuch as such techniques fail to uniformly produce the desired planarity and smoothness. Improved methods for thinning and planarizing the ~~back~~back sides of semiconductor wafers and other substrates would be desirable from the standpoint of improved process control and quality enhancement in the final product.

Please amend paragraph number **[0011]** as follows:

BRIEF SUMMARY OF THE INVENTION

[0011] The present invention comprises a method for thinning and planarization of the ~~back~~back side of semiconductor~~ substrates~~ substrates, such as semiconductor wafers. In these methods, a layer or film of highly penetrating hardenable material, hereinafter termed a "planarizing material" or a "second material" for the sake of convenience, is applied to the ~~back~~back side of a semiconductor substrate of a first material, for example, in the form of a

semiconductor wafer, to fill in valleys or "vugs" in the surface and provide a level, planar surface for subsequent thinning. The planarizing material used to coat the surface prior to thinning is selected to exhibit characteristics, when hardened, similar to those of the underlying substrate material in the exhibited rate of material removal for the particular thinning method ~~which is~~ used. Thus, for an etch-thinning method, the etch rate of the planarizing material is selected to be the same as or similar to that of the semiconductor material of the substrate. When the thinning method is mechanical abrasion (e.g., grinding, polishing), the selected planarizing material (when hardened) will exhibit the same or similar rate of solids removal as that of the semiconductor material of the substrate.

Please amend paragraph number **[0012]** as follows:

[0012] The planarizing material may comprise, for example, a polymer of any of the groups of epoxies or acrylics or, more particularly, thermal or ultraviolet (UV) cross-linkable polymer, or a two-part epoxy. Other classes of coating which may be used include silicones, urethanes and siloxanes. The relatively coarse nature of the bare wafer ~~back~~back side surface prior to backgrinding or etching to remove material enhances the penetration of the coating selected. The planarizing material may be applied prior to a first, coarse or bulk thinning operation, or following an initial or intermediate thinning step but before a final thinning or planarizing operation.

Please amend paragraph number **[0014]** as follows:

[0014] The thinning method may comprise, for example, chemical etching, mechanical (abrasive) planarization, CMP, or grinding, followed by wet or dry chemical etching. The ~~back~~back side of a wafer or die may be coated with the planarizing material at any point prior to a final planarization step.

Please amend paragraph number **[0021]** as follows:

[0021] FIG. 2 is a cross-sectional inverted side view of a portion of a semiconductor wafer following partial chemical etch planarization of the wafer ~~back~~back side by a conventional wet or dry chemical process of the prior art;

Please amend paragraph number **[0022]** as follows:

[0022] FIG. 3 is a cross-sectional inverted side view of a portion of a semiconductor wafer illustrating planarization of the wafer ~~back~~back side by mechanical grinding of the prior art;

Please amend paragraph number **[0023]** as follows:

[0023] FIG. 4 is a cross-sectional inverted side view of a portion of a semiconductor wafer showing a wafer ~~back~~back side polished to a final wafer thickness by abrasive planarization or CMP of the prior art;

Please amend paragraph number **[0025]** as follows:

[0025] FIG. 5 is a cross-sectional inverted side view of a portion of a semiconductor wafer prepared for ~~back~~back side thinning and planarization by a method of the present invention;

Please amend paragraph number **[0026]** as follows:

[0026] FIG. 6 is a cross-sectional inverted side view of a portion of a semiconductor wafer with a ~~back~~back side prepared by a method of the invention and partially thinned and planarized by a chemical etching process;

Please amend paragraph number **[0027]** as follows:

[0027] FIG. 7 is a cross-sectional inverted side view of a portion of a semiconductor wafer with a ~~back~~back side prepared by a method of the invention and thinned and planarized by mechanical grinding or abrasion or CMP to a smooth, planar surface;

Please amend paragraph number **[0031]** as follows:

DETAILED DESCRIPTION OF THE INVENTION

[0031] The prior art approach to thin a~~-substrate~~ substrate, such as a multidie semiconductor wafer~~-10~~ 10, from an initial mean thickness 18 of, e.g., about 28 mm to a final mean thickness 22 of about, e.g., 4 mm is illustrated in FIGS. 1, 2, 3, 4 and 4A. The bare ~~back~~back side surface 14 is typically rough, as shown by the exaggerated "peaks" 24 and "valleys" 26 which define the topography of the surface in FIG. 1. The roughness may be measured in terms of a maximum amplitude 38 between the deepest~~-"valley"~~ valley 26 and the highest~~-"peak"~~ peak 24. The final mean thickness 22 of semiconductor wafer 10 is shown as the distance between an active surface 12 and a final ~~back~~back side surface 20. It is very desirable that the ~~back~~back side surface 14 be as uniformly planar and smooth as possible to enable accurate and uniform severance or singulation of individual semiconductor dice cut from the semiconductor wafer 10, to maintain the structural integrity of the resulting dice and to maintain uniform thickness dimensions thereof for packaging.

Please amend paragraph number **[0033]** as follows:

[0033] As shown in FIG. 2, the etching of a bare substrate (semiconductor wafer 10) ~~surface~~ surface, such as a rough wafer ~~back~~back side surface~~-14~~ 14, reduces the topographic maximum amplitude 38 but does not planarize the etched surface 30 to a high degree due to the isotropic nature of the etch chemistry. An isotropic etchant 28 may be considered as attacking all exposed surfaces of the~~-topographic features~~ peaks and valleys 24, 26 at substantially the same rate in a direction normal to the particular surface location.

Please amend paragraph number **[0034]** as follows:

[0034] FIG. 3 depicts a movable element 32 which is moved in a lateral direction 33, such as through rotation. The movable element 32, which may be structured as a pad, carries abrasive~~-particles~~ materials 36 exposed beyond the pad surface and which impinge laterally with force against nonhorizontal ~~back~~back side surface 14, i.e., as directed lateral forces 34. A similar

effect results from use of a diamond grinding wheel. The directed lateral forces 34 tend to break the ~~"peaks"~~ peaks 24 along various crystalline cleavage planes with a resulting, significant degree of nonuniformity in the surface topography, although the amplitude will be reduced. The production of high-asperity particles from the grinding process will also be significant, leading to nonuniform solids removal.

Please amend paragraph number **[0035]** as follows:

[0035] As shown in FIG. 4, when the ~~back~~back side surface 14 of a semiconductor wafer 10 has been ground to a desired final mean thickness 22, the surface nevertheless remains undesirably rough. The valleys 26 may extend into the semiconductor wafer 10 to produce weakness therein, or even cracking or fracture. This is especially critical in very thin wafers, e.g., 2-4 mm final mean thickness 22, which are also subject to warpage. Thus, in the prior art, conventional methods may lead to failure of semiconductor dice 16 (see FIG. 4A) at the time of or following singulation from the semiconductor wafer 10, i.e., by cutting along streets 46.

Please amend paragraph number **[0036]** as follows:

[0036] Turning now to FIGS. 5 through 10, exemplary embodiments of methods of the invention are illustrated for thinning and planarizing a substrate, such as a semiconductor wafer 10 ~~back~~back side surface 14. The semiconductor wafer 10 may comprise a wafer of silicon, gallium arsenide, germanium or indium phosphide, by way of example only.

Please amend paragraph number **[0037]** as follows:

[0037] In FIG. 5, a semiconductor wafer 10 is shown with an active surface 12 and rough ~~back~~back side surface 14. A planarizing material 40 has been deposited as an overlying layer on the original nonplanar ~~back~~back side surface 14 and is shown as filling in the ~~"valleys"~~ valleys 26 and covering the ~~"peaks"~~ peaks 24 of the surface. In other words, the layer of planarizing material 40 substantially covers all features of the topography and, desirably, covers the entire ~~back~~back side surface 14. The layer of planarizing material 40 is formed and cured to have a substantially planar exposed surface 42, and is shown with a mean thickness 44. The

layer of planarizing material 40 and a substantial portion of the underlying substrate (semiconductor wafer 10) are to be removed, thinning the substrate to a final ~~wafer back~~back side surface ~~20~~ 20, which is substantially planarized.

Please amend paragraph number **[0038]** as follows:

[0038] The layer of planarizing material 40 penetrates the rough surface of ~~back~~back side surface 14 and is very adherent thereto. The planarizing material may be desirably chosen to meet the following criteria:

(a) it is easily applied to a surface of the substrate on which thinning is to be initiated;

(b) when hardened, it exhibits a solids removal rate similar to that exhibited by the underlying substrate material, e.g., semiconductor material, when subjected to the same material removal technique; and

(c) when hardened, it forms a substantially planar, exposed surface.

Please amend paragraph number **[0039]** as follows:

[0039] Materials which may be used to form the layer of planarizing material 40 of the above-listed criteria include various polymers which are in the classes of epoxies and acrylics and, more particularly, thermal (thermoset) or ultraviolet light (UV) linkable polymers and two-part epoxy formulations. Other general classes of coating which are contemplated as usable in this invention include silicones, urethanes, and siloxanes, without limitation thereto. A number of photoresists will etch at substantially the same rate as silicon materials, such as, for example, silicon dioxide. As disclosed below, it may be desirable to oxidize back side surface 14, forming silicon dioxide in the case of a silicon wafer, prior to application of the planarizing material 40. Of course, the etch rates for planarizing material 40 may be matched empirically to that of the material of the wafer for each selected etchant.

Please amend paragraph number **[0040]** as follows:

[0040] The application of a layer of planarizing material 40 to a substrate ~~back~~back side surface 14 may be by a variety of methods. In one method for example, a flowable polymeric

material (liquid or particulate solid) may be applied to a ~~back~~back side surface 14 by screen-coating or stencil-coating. If a liquid material is used, spin-coating is also effective. The polymeric material may then be cured to a hardened state by application of heat or, in some instances, by a selected wavelength of radiation. In another variation, an epoxy material can be cured to a so-called "B" stage of tackiness, at which it is still flowable. The epoxy material may then be applied to the ~~back~~back side surface 14 and reheated to complete the cure, bond to the surface and harden. It is contemplated that a layer of epoxy material may be applied to a backing sheet carrying a release layer, cured to a "B" stage and applied to the ~~back~~back side surface 14. The backing may then be stripped off, and the epoxy cure and hardening completed.

Please amend paragraph number **[0042]** as follows:

[0042] In a deposition method of newer development, the Parylene Process ™ may be used. In this method, an organic dimer is heated to form monomers and then applied at a lower temperature to a ~~back~~back side surface 14 where it deposits as ~~a polymeric layer~~ planarizing material 40. A dimer such as di-para-xylene may be used.

Please amend paragraph number **[0043]** as follows:

[0043] Another deposition method which may be used comprises the formation of a tape or film element of partially polymerized material. The tape or film may then be applied to the ~~back~~back side surface 14, heated to flow, bond to the surface, level and planarize, and finally cooled to a solid state.

Please amend paragraph number **[0044]** as follows:

[0044] FIG. 6 shows the substrate (semiconductor wafer 10) of FIG. 5 following exemplary thinning by wet or dry chemical etching by isotropic etchant 28 to produce an etched surface 30 ~~which is~~ near the original ~~back~~back side surface 14. Unlike the rough original ~~back~~back side surface 14, the etched surface 30 is substantially planar and includes etched portions of the planarizing material 40. The exposure to isotropic etchant 28 may be continued until the desired final ~~wafer back~~back side surface 20, i.e., ~~wafer~~ final mean thickness 22, is

reached. Inasmuch as the planar exposed surface 42 initially exposed to the isoctropic etchant 28 is substantially planar, the ~~finally~~ attained final ~~back~~back side surface 20 will also be substantially planar. While dry etching, for example, reactive ion etching (also termed "plasma etching"), may be used to thin a substrate, it is currently preferred that wet etching be employed. Suitable etchants for a silicon substrate include, without limitation, 100% KOH, KOH mixed with deionized water, KOH mixed with isopropyl alcohol, a mixture of HF, HNO_3 and CH_3COOH formulated, for example as so-called "95% poly etch," comprising 50% nitric acid, 2.5% acetic acid and 0.74% hydrofluoric acid, by volume.

Please amend paragraph number **[0045]** as follows:

[0045] However, a mechanical or chemical-mechanical material removal process may be used to thin the ~~back~~back side surface 14. As shown in FIG. 7, a movable element 32 with attached abrasive ~~particles~~ materials 36 may be used to grind a substrate (semiconductor wafer 10) to (or nearly to) a desired final ~~desired~~ mean thickness 22. The movable element 32 may be moved in a lateral direction or lateral directions 33 parallel to the desired final ~~substrate~~ ~~back~~back side surface 20 to remove substrate material until surfaces 14 and 20 merge.

Please amend paragraph number **[0046]** as follows:

[0046] The acts of the methods of the present invention may be conducted in differing orders. As shown in FIG. 8 with respect to one exemplary embodiment, a substrate is provided in act 50 with a bare, thinnable ~~back~~back side surface 14. The term "bare" denotes that electronic or other components are not present on the ~~back~~back side surface 14. A layer of planarizing material 40 is then applied, as discussed above, in act 52. Following hardening in act 54, one or more thinning and planarizing acts 58 may be used to thin and complete planarization. The thinning and planarization acts 58 may be of any of the previously mentioned techniques.

Please amend paragraph number **[0048]** as follows:

[0048] FIG. 10 illustrates another exemplary embodiment of a method of the present invention. In this embodiment, the thinnable ~~backback~~back side surface 14 is first subjected to an oxidation act 60. When the substrate is silicon, for example, the ~~backback~~back side surface 14 may be oxidized to silicon dioxide. Polymers such as are used as planarizing materials in this invention are, in general, much more adherent to the oxide than to silicon itself. However, it should be noted that, in general, the initially rough ~~backback~~back side surface 14 may enhance adhesion of such a polymer thereto and render preoxidation in act 60 unnecessary.